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PROCESS FOR FORMING AN OXIDE LAYER OF NON-UNIFORM THICKNESS ON THE SURFACE OF A SILICON SUBSTRATE

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The present invention relates in general to a process for forming a silicon oxide layer and more particularly a silicon oxide layer of non-uniform thickness on the surface of a silicon substrate.

In microelectronics, the gate oxide layer, which is a fundamental element of many semiconductor devices such as MOS transistors, is becoming thinner and thinner. Thus, in 0.18 μm technology, thicknesses of less than 4 nm are required for the gate oxide layer. This reduction in thickness of the gate oxide layer necessarily leads to a reduction in the supply voltages of the devices so as to prevent premature degradation of the gate oxide layer. In the case of microprocessors, it is not always possible to reduce the supply voltage, because of the input/output buses (I/O buses) which require higher voltages. To solve this problem, silicon oxide layers of different thicknesses have been grown on predetermined regions of the same silicon substrate, the thickest oxide layers being formed at points where the voltages applied will be the highest.

In order to obtain, on a surface of the same silicon substrate, a silicon oxide layer having two different thicknesses in predetermined regions of the surface of the substrate, a two-step oxidation process has been used.

The first step of the process ~~consists in~~ includes growing a first layer of silicon oxide of uniform thickness by oxidation on the surface of the substrate.

The second step ~~consists in~~ includes growing a second silicon oxide layer by oxidation, but with masking of predetermined regions of the surface of the substrate that have already been covered with the first oxide layer, in order in this way to obtain a final oxide

layer of greater thickness in the unmasked regions.

The major drawback of this process is the contamination of the gate oxide during the masking and etching steps.

To remedy the drawbacks of the above masking process, a process has recently been proposed in which a non-uniform thickness oxide layer is grown in a single step. This process ~~consists in~~ includes forming, on the surface of the substrate, predetermined regions having an oxidation rate reduced by nitrogen ion implantation in these predetermined regions, at points where it is desired to obtain a thinner oxide layer, and then in growing a silicon oxide layer by oxidation of the surface of the silicon substrate. Such a process is described, other others, in the article "Formation of Ultrathin Nitrided SiO_2 Oxides by Direct Nitrogen Implantation into Silicon", by H.R. Soleimani, B.S. Doyle and A. Philipossian, J. Electrochem. Soc., Vol. 142, No. 8, August 1998.

The latter process also has serious drawbacks since the high dose of implanted nitrogen ($>10^{15}$ cm^{-2}) inevitably leads to degradation of the thin gate oxide layer. This drawback is all the more problematic when the implanted regions are in the majority on the substrate and the thinner the oxide layer is thereon (and therefore the more sensitive it is to degradation problems).

~~The subject of the present invention is therefore~~ a process for growing a silicon oxide layer of non-uniform thickness on a surface of a silicon substrate which remedies the drawbacks of the processes of the prior art.

~~According to the invention, the process is characterized in that it comprises the following steps:~~

a) implantation in predetermined regions of the substrate of an effective dose of atoms of a chemical species which increases the rate of oxidation of the substrate; and

b) the growth of a silicon oxide layer of non-uniform thickness by oxidation on the surface of the substrate.

The implantable species which increase the rate of oxidation of a silicon substrate comprise silicon, germanium, argon, neon, helium, phosphorus and arsenic. The preferred species are Si, Ge, Ar, Ne and He and more preferred Si, Ge and Ar.

Although the implantation of phosphorus or arsenic increases the rate of oxidation of a silicon substrate, these species have the drawback, however, of being dopants of silicon which modify its electrical properties, something which is not always desirable.

Increasing the oxidation rate of a silicon substrate obviously depends on the nature of the chemical species implanted, on the implanted dose and on the implantation energy. In general, the dose of chemical species implanted will vary between 5×10^{13} and 5×10^{15} atoms/cm^2, preferably from 1×10^{15} to 5×10^{15} atoms/cm^2.

The implantation energy may vary from less than 2 keV to more than 100 keV, but is generally from 2 to 80 keV and preferably from 2 to 15 keV.

The implantation of atoms of a chemical species into a silicon substrate is conventional and well known in the art. Thus, it is possible to use a process and an apparatus for conventional ion implantation in which the chemical species to be implanted is ionized before being accelerated by means of an electric field.

A conventional apparatus for carrying out such an implantation is the SHC 80-type VARIAN apparatus.

The process ~~of the invention~~ can be used with any type of silicon substrate, whether crystalline, polycrystalline or amorphus.

The step of growing the silicon oxide layer is conventional and may be carried out by oxidation in a standard furnace at a temperature above 300°C and in an oxidizing atmosphere, such as oxygen, diluted oxygen, water vapor, ozone or other gases. It is also possible

to use other conventional oxidation processes such as plasma oxidation, electrochemical oxidation and rapid thermal oxidation (RTO).

EXAMPLE

A silicon oxide layer was grown on silicon wafers by thermal oxidation in a standard furnace (SVG brand) at a temperature of 900°C for 6 minutes in an oxygen atmosphere.

Some of the wafers were subjected beforehand to argon ion implantation in a similar manner but with different implantation energies (VARIAN SHC 80 implantation apparatus).

The thickness of the silicon oxide layers obtained was measured by ellipsometry. The results are given in Table I below.

Sub B2

TABLE I

Implantation energy / Implanted dose	2 keV	10 keV	80 keV
5×10^{13} at/ cm^2	4.78	5.74	-
5×10^{14} at/ cm^2	5.66	5.92	6.0
1×10^{15} at/ cm^2	6.01	6.75	-
5×10^{16} at/ cm^2	8.8	12.3	11.0

By way of comparison, the thickness of the oxide layer obtained under the same oxidation conditions on a similar silicon wafer that has not undergone oxidation is 4.7 nm.

Ne or He implantation leads to the same results as argon.

Phosphorus and arsenic implantation, with an energy of 10 keV and with implantation does of 2×10^{15} atoms/cm^2 and 3×10^{15} atoms/cm^2 respectively, have led to 12 and 17 nm oxide layers, respectively.

Because the process according to the invention is based on increasing the oxidation rate of a silicon substrate and not on reducing this rate, which is the case in the prior art, the risk of degrading the regions in which the oxide layer is thinnest is eliminated, while at the same time obtaining oxide layers of greater thicknesses suitable for withstanding higher voltages, for example at the I/O buses.